# 512K x 8 HIGH-SPEED CMOS STATIC RAM

**FEBRUARY 2003**

## FEATURES

- High-speed access times:
  10, 12 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- $\overline{CE}$ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- Packages available:
  – 36-pin 400-mil SOJ
  – 36-pin miniBGA
  – 44-pin TSOP (Type II)

## DESCRIPTION

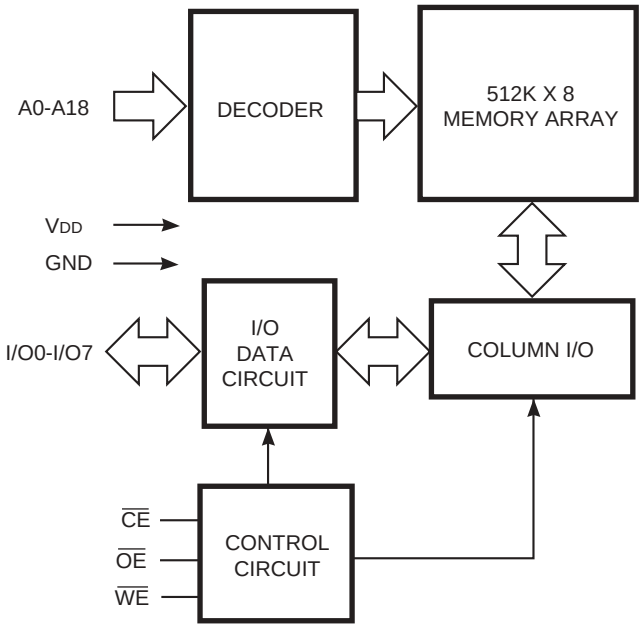
The *ISSI* IS61LV5128AL is a very high-speed, low power, 524,288-word by 8-bit CMOS static RAM. The IS61LV5128AL is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) with CMOS input levels.

The IS61LV5128AL operates from a single 3.3V power supply and all inputs are TTL-compatible.

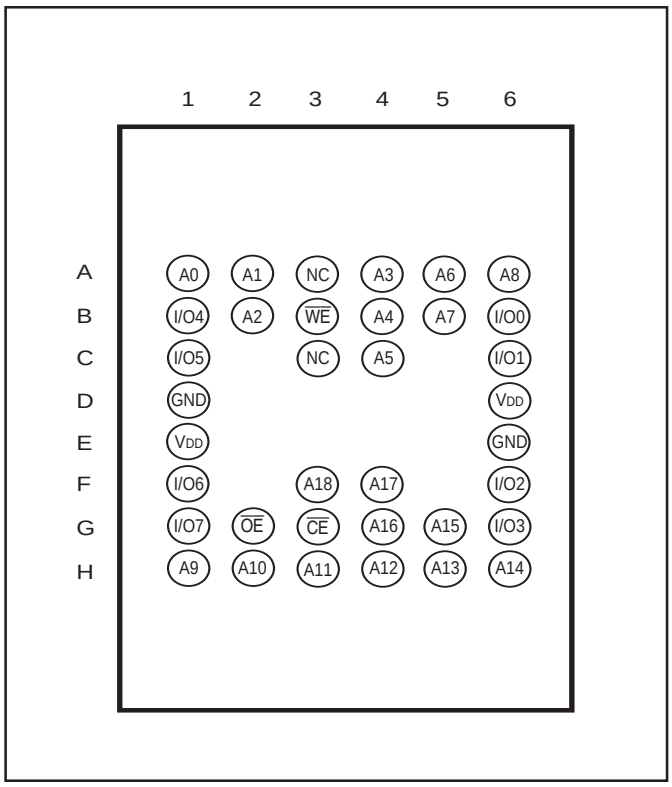
The IS61LV5128AL is available in 36-pin 400-mil SOJ, 36-pin mini BGA, and 44-pin TSOP (Type II) packages.

## FUNCTIONAL BLOCK DIAGRAM

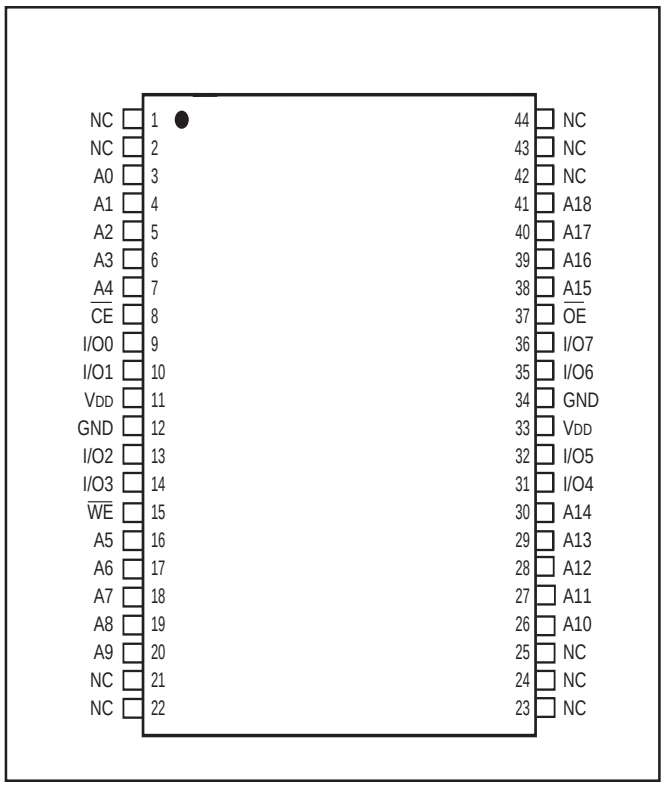


## PIN CONFIGURATION

### 36 mini BGA



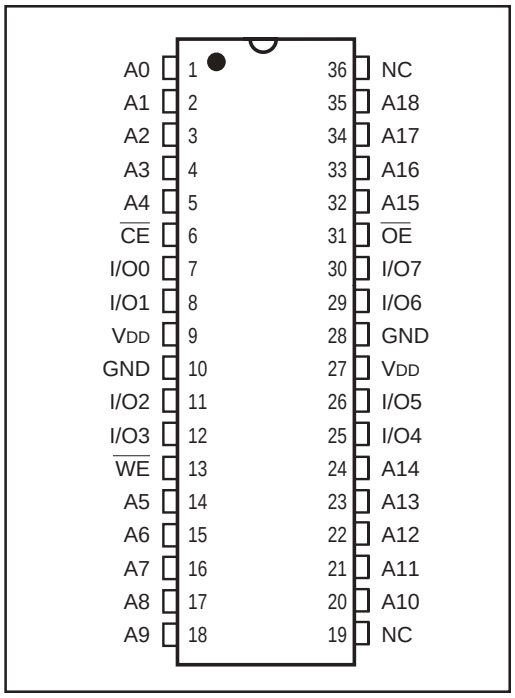

### 44-Pin TSOP (Type II)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A18 | Address Inputs |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{WE}$ | Write Enable Input |
| I/O0-I/O7 | Bidirectional Ports |
| $V_{DD}$ | Power |
| GND | Ground |
| NC | No Connection |

### 36-Pin SOJ




## TRUTH TABLE

| Mode | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | I/O Operation | $V_{DD}$ Current |
|---|---|---|---|---|---|
| Not Selected (Power-down) | X | H | X | High-Z | $I_{SB1}$, $I_{SB2}$ |
| Output Disabled | H | L | H | High-Z | $I_{CC}$ |
| Read | H | L | L | $D_{OUT}$ | $I_{CC}$ |
| Write | L | L | X | $D_{IN}$ | $I_{CC}$ |

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to $V_{DD}$ + 0.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |

**Notes:**
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

| | | $V_{DD}$ | |
|---|---|---|---|
| Range | Ambient Temperature | 10ns | 12ns |
| Commercial | 0°C to +70°C | 3.3V +10%, -5% | 3.3V ±10% |
| Industrial | -40°C to +85°C | 3.3V +10%, -5% | 3.3V ±10% |

## CAPACITANCE(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{OUT}$ = 0V | 8 | pF |

**Notes:**
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = 3.3V.

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{DD}$ = Min., $I_{OH}$ = –4.0 mA | | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = Min., $I_{OL}$ = 8.0 mA | | — | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND ≤ $V_{IN}$ ≤ $V_{DD}$ | Com.<br>Ind. | –2<br>–5 | 2<br>5 | µA |
| $I_{LO}$ | Output Leakage | GND ≤ $V_{OUT}$ ≤ $V_{DD}$, Outputs Disabled | Com.<br>Ind. | –2<br>–5 | 2<br>5 | µA |

**Note:**
1. $V_{IL}$ = –3.0V for pulse width less than 10 ns.

## POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

| | | | | -10 | | -12 | | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Test Conditions | | Min. | Max. | Min. | Max. | Unit |
| $I_{CC}$ | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}$ = Max.,<br>$I_{OUT}$ = 0 mA, f = $f_{MAX}$ | Com.<br>Ind. | —<br>— | 90<br>95 | —<br>— | 85<br>90 | mA |
| $I_{SB}$ | TTL Standby Current (TTL Inputs) | $V_{DD}$ = Max.,<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\overline{CE}$ ≥ $V_{IH}$, f = $f_{MAX}$. | Com.<br>Ind. | —<br>— | 40<br>45 | —<br>— | 35<br>40 | mA |
| $I_{SB1}$ | TTL Standby Current (TTL Inputs) | $V_{DD}$ = Max.,<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\overline{CE}$ ≥ $V_{IH}$, f = 0 | Com.<br>Ind. | —<br>— | 20<br>25 | —<br>— | 20<br>25 | mA |
| $I_{SB2}$ | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = Max.,<br>$\overline{CE}$ ≥ $V_{DD}$ – 0.2V,<br>$V_{IN}$ ≥ $V_{DD}$ – 0.2V, or<br>$V_{IN}$ ≤ 0.2V, f = 0 | Com.<br>Ind. | —<br>— | 15<br>20 | —<br>— | 15<br>20 | mA |

**Note:**
1. At f = $f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

## READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

| Symbol | Parameter | -10 Min. | -10 Max. | -12 Min. | -12 Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 10 | — | 12 | — | ns |
| $t_{AA}$ | Address Access Time | — | 10 | — | 12 | ns |
| $t_{OHA}$ | Output Hold Time | 2 | — | 2 | — | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | — | 10 | — | 12 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | — | 4 | — | 5 | ns |
| $t_{HZOE}$[2] | $\overline{OE}$ to High-Z Output | — | 4 | — | 5 | ns |
| $t_{LZOE}$[2] | $\overline{OE}$ to Low-Z Output | 0 | — | 0 | — | ns |
| $t_{HZCE}$[2] | $\overline{CE}$ to High-Z Output | 0 | 4 | 0 | 6 | ns |
| $t_{LZCE}$[2] | $\overline{CE}$ to Low-Z Output | 3 | — | 3 | — | ns |
| $t_{PU}$ | Power Up Time | 0 | — | 0 | — | ns |
| $t_{PD}$ | Power Down Time | — | 10 | — | 12 | ns |

**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage.

## AC TEST CONDITIONS

| Parameter | Unit |
|---|---|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

## AC TEST LOADS

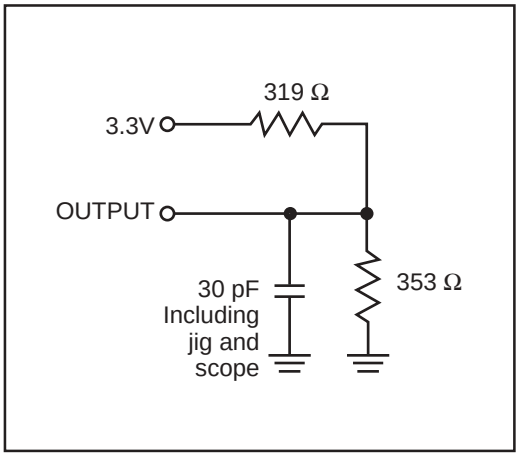



**Figure 1**

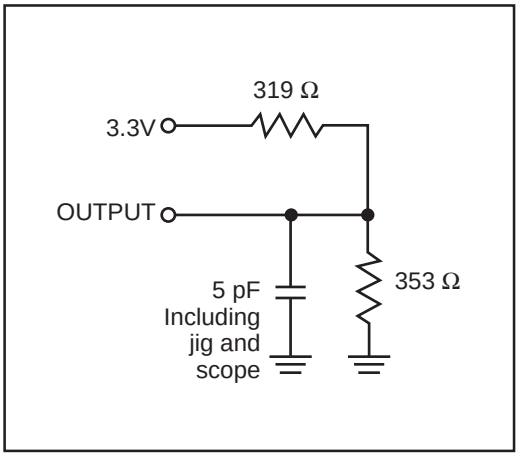
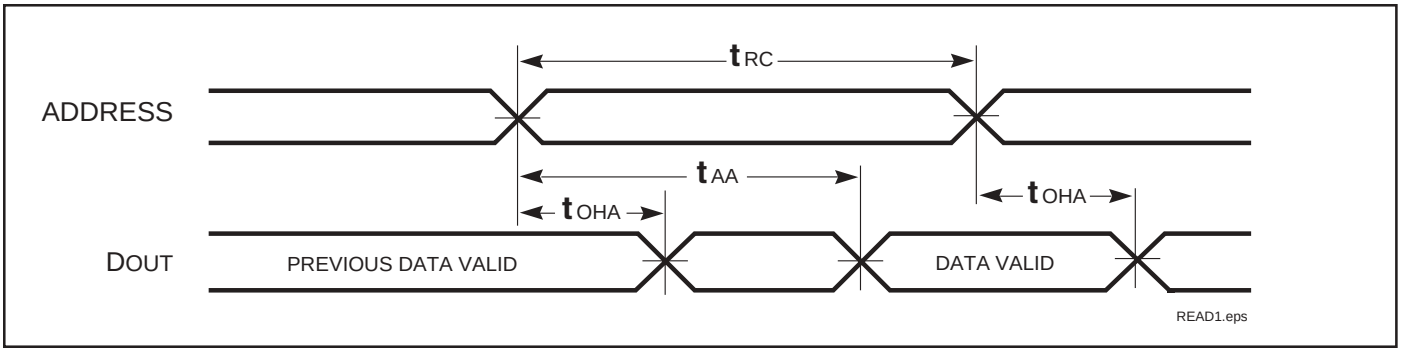


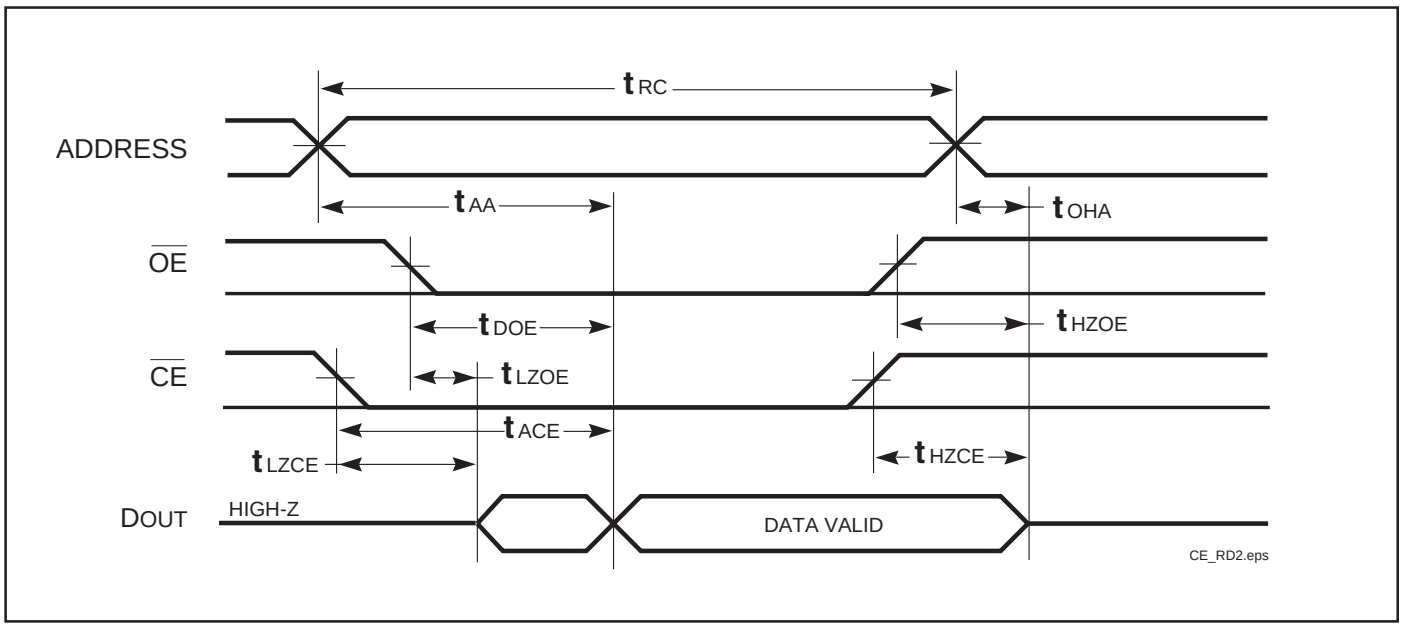

**Figure 2**

## AC WAVEFORMS

### READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CE}$ = $\overline{OE}$ = $V_{IL}$)




### READ CYCLE NO. 2[1,3] ($\overline{CE}$ and $\overline{OE}$ Controlled)




**Notes:**
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

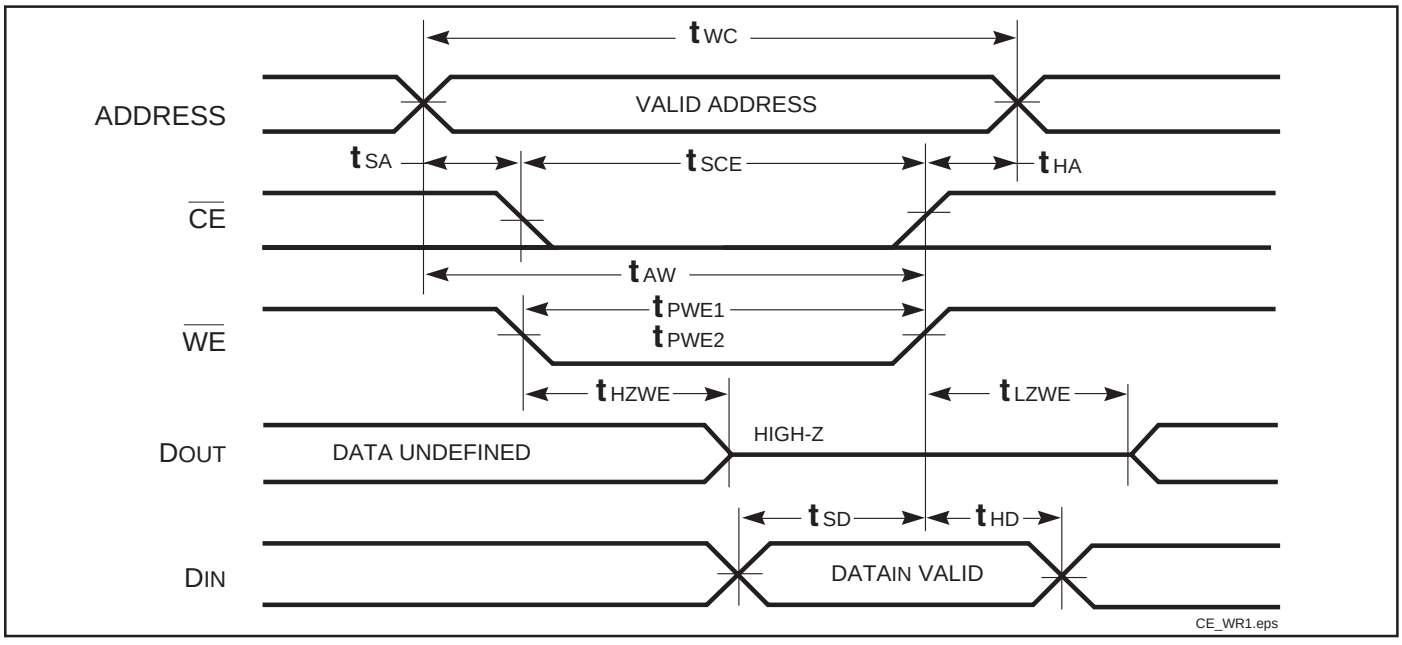
## WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

| Symbol | Parameter | -10 Min. | -10 Max. | -12 Min. | -12 Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time | 10 | — | 12 | — | ns |
| $t_{SCE}$ | $\overline{CE}$ to Write End | 8 | — | 8 | — | ns |
| $t_{AW}$ | Address Setup Time to Write End | 8 | — | 8 | — | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | — | 0 | — | ns |
| $t_{SA}$ | Address Setup Time | 0 | — | 0 | — | ns |
| $t_{PWE1}$ | $\overline{WE}$ Pulse Width | 8 | — | 8 | — | ns |
| $t_{PWE2}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW) | 10 | — | 12 | — | ns |
| $t_{SD}$ | Data Setup to Write End | 6 | — | 6 | — | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | — | 0 | — | ns |
| $t_{HZWE}$[2] | $\overline{WE}$ LOW to High-Z Output | — | 5 | — | 6 | ns |
| $t_{LZWE}$[2] | $\overline{WE}$ HIGH to Low-Z Output | 2 | — | 2 | — | ns |

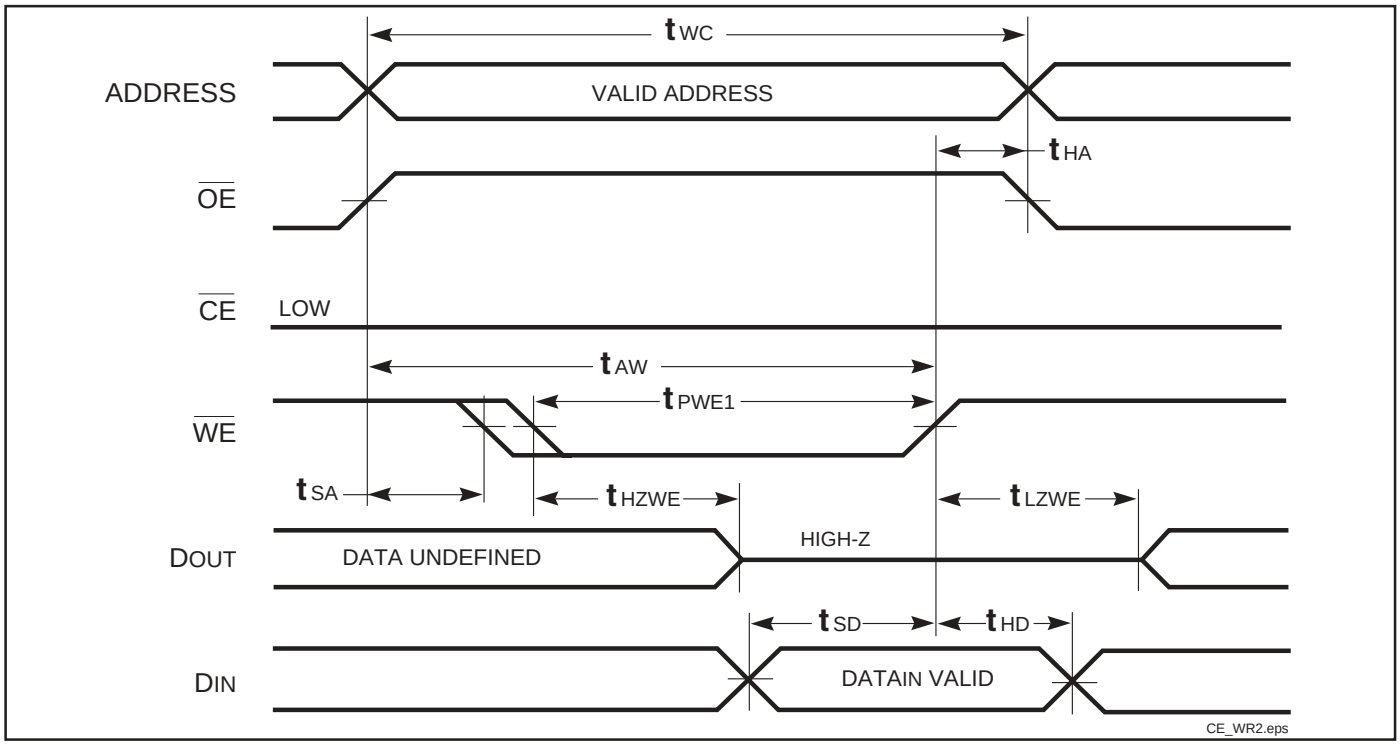
**Notes:**
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

## AC WAVEFORMS

### WRITE CYCLE NO. 1[1,2] ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

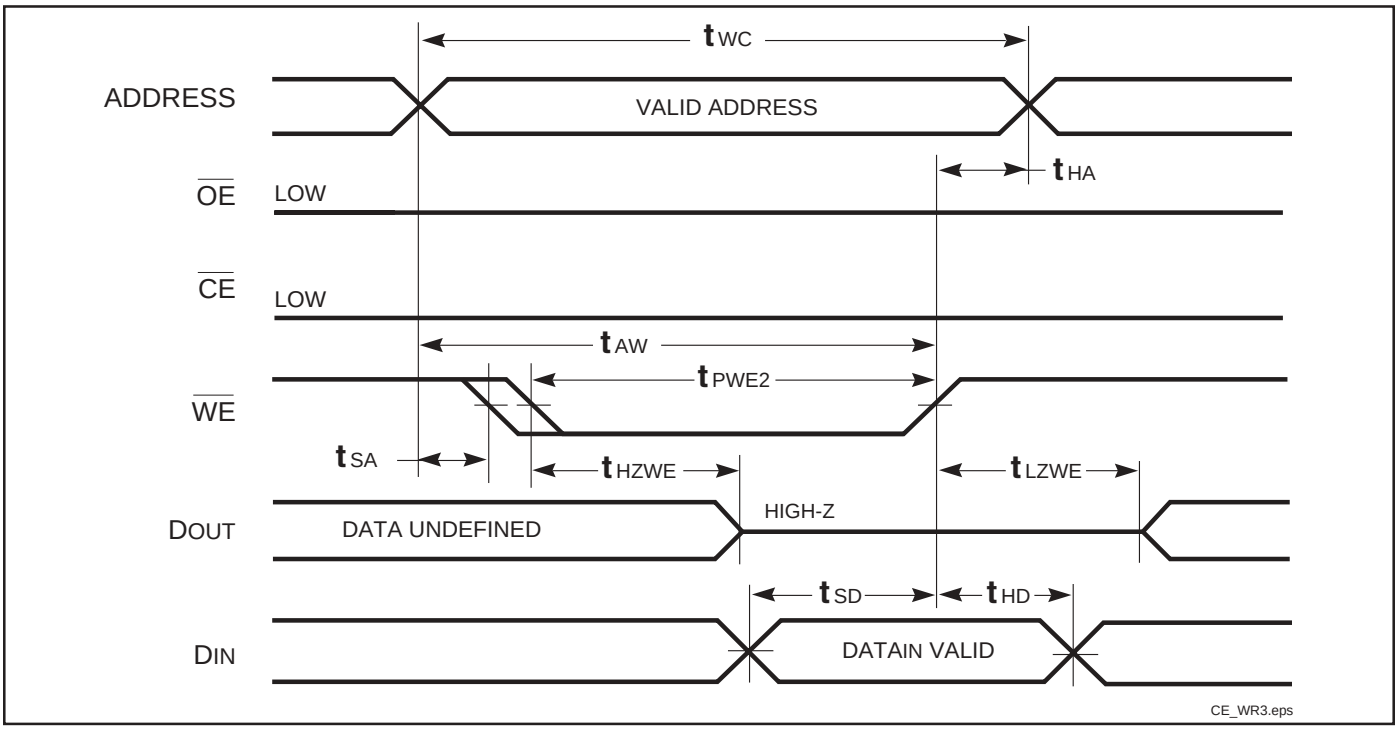


## WRITE CYCLE NO. 2[1,2] ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)




**Notes:**
1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ > $V_{IH}$.

## WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



## ORDERING INFORMATION

### Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 10 | IS61LV5128AL-10K | 400-mil Plastic SOJ |
| 10 | IS61LV5128AL-10T | TSOP (Type II) |
| 10 | IS61LV5128AL-10B | mini BGA (8mmx10mm) |
| 12 | IS61LV5128AL-12K | 400-mil Plastic SOJ |
| 12 | IS61LV5128AL-12T | TSOP (Type II) |

### Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 10 | IS61LV5128AL-10KI | 400-mil Plastic SOJ |
| 10 | IS61LV5128AL-10TI | TSOP (Type II) |
| 10 | IS61LV5128AL-10BI | mini BGA (8mmx10mm) |
| 12 | IS61LV5128AL-12KI | 400-mil Plastic SOJ |
| 12 | IS61LV5128AL-12TI | TSOP (Type II) |